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EXAMINER	
SINGH, DALIP K	

ART UNIT	PAPER NUMBER
2628	

DATE MAILED: 10/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/822,013	DIAMOND ET AL.	
	Examiner	Art Unit	
	Dalip K. Singh	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-54* is/are pending in the application.

4a) Of the above claim(s) *1-15 and 40-42* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-39 and 43-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11-14-2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's election of claims 16-39 with addition of new dependent claims 43-54 and withdrawl of claims 1-15 and 40-42 as non-elected claims as per the Restriction Requirement of June 28, 2005 is acknowledged as per the reply filed on July 28, 2005. The subsequent Restriction Requirement of October 19, 2005 is being withdrawn. The status of claims after this Office Action: original claims 16-39; addition of new dependent claims 43-54; and withdrawl of claims 1-15 and 40-42 as non-elected claims

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 16, 17, 24, 44, 46, and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,724,389 B1 to Wilen et al. in view of US 6,202,039 B1 to Finger.

a. Regarding claim 16, Wilen et al. **discloses** a motherboard (computer system 100, Fig. 1); a central processing unit (processor 110, Fig. 1) mounted to the motherboard (computer system 100);an integrated graphics processor (IGP) (on-board accelerated graphics port (AGP) device 150, Fig. 1) mounted to the motherboard (computer system 100); a connector (AGP connector 152, Fig. 1) a field-changeable rendering card (external AGP device 154, Fig. 1) interfaced to the motherboard (computer system 100), wherein the field-changeble graphics card resides in an independent, spaced-apart relation relative to the motherboard (...the external AGP device 154 is an add-on...located

externally to the motherboard...The ADD card 156 is a graphics device that interfaces the AGP connector 152...col. 3, lines 34-39). Further, Wilen et al. **discloses** a strapping scheme that indicates the presence of ADD card 156 at the AGP connector housing (...One way to do this is to use a pull-up resistor at the PAR signal....To indicate that an ADD card is used, the aDD card pulls this signal LOW...col. 6, lines 49-52;...the configuration signals ADD_ID0 to ADD_ID7 are strapped to high or low depending on the configuration of the ADD card 156...col. 6, lines 60-62;...A detector pin strappable to a logic level to indicate an external graphics card is used...Abstract). Further, Wilen et al. **discloses** on-board and external TMDS/LVDs devices that can drive a flat panel display or a digital display (...the on-board and external TMDS/LVDS devices 140 and 142 are graphic devices that interface to the DVO signaling from the interface port 130. The on-board TMDS/LVDS device 140 is located on the motherboard containing the processor 110 while the external TMDS/LVDS 142 is an add-on card to be plugged into a slot having interface to the interface port 130. The TMDS/LVDS devices 140 and 142 drive a flat panel display or a digital display monitor through a TMDS/LVDS transmitter...col. 3, lines 10-25). Wilen et al. **further discloses** use of pull-up resistor to identify whether an external graphics card or the internal AGP card is in use and thus accordingly configuring output display panels (col. 6, lines 43-67). Wilen et al. **discloses** interface port 130 that interfaces to a number of devices, i.e., DVI, (TMDS or LVDS devices) and television set 144 (...the interface port 130 provides connection pins to interface to a number of devices....In one embodiment, these graphic mode includes a DVO mode and an AGP mode. The DVO mode may include a digital visual interface (DVI)...col. 2, lines 60-67; col. 3, lines 1-4;...The TMDS/LVDS devices 140 and 142 drive a flat panel display or a digital display monitor through a TMDS/LVDS transmitter...col. 3, lines 15-18). *Looking at the specification of instant application on page 7, paragraphs 0030 and*

0032 "In one embodiment, graphics system 600 further comprises a plurality of stuffing resistors 614a and 614b(shown in phantom) adapted for completing the circuits from IGP 612 and from loop-through card 650 to display panels 604-610. During assembly of a computing system, a manufacturer may configure graphics system 600 to operate in the mode described (e.g., incorporating loop-through card 650) by closing the circuit paths through resistors 614a and leaving the circuit paths through resistors 614b open...paragraph 0030; As described above, stuffing resistors 614b complete the circuits from graphics card 660 to display panels 604-610".

Therefore, interfacing plurality of display panels is done by stuffing resistors as per the claim limitations and as supported in the specification. However, Wilen et al. **does not explicitly disclose** a plurality of stuffing resistors adapted for interfacing the field-changeble graphics card to a plurality of output display panels. Finger **discloses** a device for driving selected display devices based on arbitrary input parameters (...It is intended that one and only one chip serve all the instrumentation needs of a product line that will operate from numerous power sources, with innumerable transducers, displaying numerous transforms in either LED or LCD formats, with many functional options...Therefore, it is desirable that the invention will be programmable at the chip level via non-volatile memory, and at the circuit board level via "stuffing" instructions. Typical stuffing instructions will be resistor values for voltage options. Resistor values for classes of transducers, capacitor values for filter response, LED arrays for specific color formats, LCD assemblies for specific legend, etc...col. 3, lines 52-63). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Wilen with the feature "stuffing options of using resistors" as taught by Finger **because** it provides for cheaper method of configuring a display interface option i.e., use of resistors.

b. Regarding claim 17, Wilen et al. **discloses** a connector (AGP connector 152, Fig. 1) for attaching field-changeable graphics card (...the external AGP device 154 is an add-on...located externally to the motherboard...The ADD card 156 is a graphics device that interfaces the AGP connector 152...col. 3, lines 34-39) (external AGP device 154, Fig. 1) to the motherboard (computer system 100), the connector comprising a plurality of connector pins (...The AGP connector 152 is a connector that supports the AGP standard (e.g., version 2.0)...col. 3, lines 25-35).

c. Regarding claim 24, Wilen et al. **discloses** wherein the field-changeble graphics card is an active graphics card comprising a graphics processing unit (GPU) (...the external AGP device 154 is an add-on...graphics device located externally to the motherboard...col. 3, lines 34-40).

d. Regarding claim 44, Wilen et al. **discloses** ADD_Detect signal on one of connector pins to identify that the ADD card 156 (Fig. 1) is used instead of the AGP card 154 (col. 6, lines 43-45).

e. Regarding claim 46, Wilen et al. **discloses** a detector pin strappable to a logic level to indicate an external graphics card being used in the first graphics mode (Abstract).

f. Regarding claim 47 , Wilen et al. **discloses** the interface port 130 including multiplexed pins to support at least two graphics modes (..the interface port 130 provides connection pins to interface to a number of devices. The interface port 130 includes multiplexed pins to support at least two graphics modes...col. 2, lines 62-65). Further, Wilen makes use of logic levels using a pull-up resistor. When an ADD card is used, the ADD card pulls this signal LOW (...The ADD_Detect signal is used to identify that the ADD card 156 (Fig. 1) is used instead of the AGP card 54...One way to do this is use a pull-up resistor at the PAR signal...To indicate that an ADD card is used, the ADD

card pulls this signal LOW. When this occurs, the integrated chipset 205 disables the PCI configuration register #1 (host to AGP bridge). This causes the integrated chipset to behave as if it had no AGP interface and will not attempt to initialize the AGP mode. A system that does not use the integrated chipset 205 and uses a MCH only will ignore the ADD card 156 according to the AGP Specification 2.0...col. 6, lines 43-59).

4. Claims 43 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,724,389 B1 to Wilen et al. in view of US 6,202,039 B1 to Finger as applied claim 16 above, and further in view of US 6,731,514 B2 to Evans.

a. Regarding claim 43, Wilen-Finger combination **does not disclose** wherein the connector is further adapted to maintain a graphics card in a substantially parallel, spaced apart relation relative to the motherboard. Evans **discloses** in FIG. 1 a single module. The module comprises a support plate 2 (for example in the form of a printed circuit board) which, as can be seen in plan view in FIG. 2, is rectangular in shape and essentially planar. Two through-holes 4 are formed in the plate. The plate 2 carries on its upper surface or topside a set of electrical components labeled 6 in FIG. 1. The topside of the plate 2 also carries a support pillar 8, which is an essentially cylindrical pillar having two diameters interfacing to form a stepped portion 10, the purpose of which will be discussed later. A connector space clearance component 12 is also provided on the topside of the plate. (col. 3, lines 9-20). FIG. 3 illustrates a modular system comprising a main board 50 and a plurality of modules M0, M1. Although only two modules are shown in FIG. 3, it will be apparent that any number of modules may be provided. (8) The main board 50 in the described embodiment comprises a printed circuit board for a set top box. It carries a plurality of main board components 22 including the main processor 40, and a main board interface connector 24 mounted to its topside. The main board interface connector 24 is of the same type as the pass

through connector 14 on each module. The main board 50 also carries a support pillar 26 and has two through holes 28. Reference numeral 30 denotes a system case panel which abuts the connector space clearance component 12. As can readily be seen in FIG. 3, the interface connector 18 on the underside of a module engages the pass through connector 14 on the topside of the lower module. A support pillar 8 of the lower module extends through each of the through holes 4 of the module above it and engages with its stepped portion 10 the underside of the support pillar 8 of the upper module to form a continuous support arrangement (col. 3, lines 60-67; col. 4, lines 1-14). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught Wilen-Finger combination with the feature "connector adapted to maintain a graphics card in a substantially parallel, spaced apart relation relative to the motherboard" as taught by Evans **because** stackable module provide expansion capabilities and this way it minimizes motherboard requirements.

b. Regarding claim 45, Wilen-Finger combination **does not disclose** wherein the connector is a right-angle edge connector. Evans **discloses** wherein the connector is a right-angle edge connector mounted to the motherboard (See Fig. 1, and Fig. 3, element 18; Evans). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Wilen-Finger combination with the Evans teaching of right-angle edge connector as it provides expansion capabilities and minimizes motherboard requirements.

5. Claims 18-23, and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,724,389 B1 to Wilen et al. in view of US 6,202,039 B1 to Finger as applied claim 16 above, and further in view of US 6,555,745 B1 to Kruse et al.

a. Regarding claim 18, Wilen-Finger combination **is silent about** wherein said field-changeable card is a passive loop-through card. The detailed specification of the

instant application discloses how the loop-through card 650 completes the circuit paths between the output signals and LVDS panel input signals (paragraph 0030). Kruse et al. **discloses** a flexible interconnect arrangement (FIA) facilitating low voltage differential signal communications between an analyzer and a display screen with a highly flexible, high impedence circuit board (col. 2, line 64-67), which acts as a loop-through card. Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Wilen-Finger combination with the feature "loop-through for passing data" as taught by Kruse et al. **because** it provides for a reduced electromagnetic interference operations resulting in improved operations.

b. Regarding claim 19, Wilen-Finger combination **discloses** a strapping scheme that indicates the presence of ADD card 156 at the AGP connector housing (...One way to do this is to use a pull-up resistor at the PAR signal....To indicate that an ADD card is used, the aDD card pulls this signal LOW...col. 6, lines 49-52;...the configuration signals ADD_ID0 to ADD_ID7 are strapped to high or low depending on the configuration of the ADD card 156...col. 6, lines 60-62;...A detector pin strappable to a logic level to indicate an external graphics card is used...Abstract). Further, Wilen et al. **discloses** on-board and external TMDS/LVDS devices that can drive a flat panel display or a digital display (...the on-board and external TMDS/LVDS devices 140 and 142 are graphic devices that interface to the DVO signaling from the interface port 130. The on-board TMDS/LVDS device 140 is located on the motherboard containing the processor 110 while the external TMDS/LVDS 142 is an add-on card to be plugged into a slot having interface to the interface port 130. The TMDS/LVDS devices 140 and 142 drive a flat panel display or a digital display monitor through a TMDS/LVDS transmitter...col. 3, lines 10-25). However, Wilen-Finger combination **does not disclose** use of of the passive loop-through card to an output display panel. Kruse et al. **discloses** a flexible

interconnect arrangement (FIA) facilitating low voltage differential signal communications between an analyzer and a display screen with a highly flexible, high impedence circuit board (col. 2, line 64-67), which acts as a loop-through card. Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Wilen-Finger combination with the teachings of Kruse et al. to make use of flexible interconnect arrangement (FIA) similar to a loop-through feature **because** it results in providing the LVDS connectivity without incurring the costs of LVDS drivers resulting in cost savings.

c. Regarding claim 20, Wilen-Finger combination **does not disclose** wherein the connector is adapted to cause an LVDS signal to be routed through the loop-through card to the output device comprising a display. Kruse et al. **discloses** wherein the connector is adapted to cause an LVDS signal to be routed through the loop-through card to the output device comprising a display (...a first end 102 of flexible interconnect arrangement 100 connects to the display screen via a connector 103. A second end 104 connects to the analyzer of the programming unit via a connector 105...col. 3, lines 20-40), the loop-through card being a conduit for passing the signals through without any processing to the display. Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Wilen-Finger combination with the teachings of Kruse et al. to make use of flexible interconnect arrangement (FIA) similar to a loop-through feature **because** it results in providing the LVDS connectivity without incurring the costs of LVDS drivers resulting in cost savings.

d. Regarding claim 21, Wilen et al. **discloses** support for both DVO as well as AGP outputs, and since it is a stuffing option, it would have to be set up for usage by the end user and supports other graphics modes (...Wilen is directed to the digital video output

(DVO) and accelerated graphics port (AGP) graphics modes, it can be practiced for other graphics modes having similar characteristics...col. 2, lines 5-10).

e. Regarding claim 22, Wilen et al. **discloses** a strapping scheme that indicates the presence of ADD card 156 at the AGP connector housing (...One way to do this is to use a pull-up resistor at the PAR signal....To indicate that an ADD card is used, the aDD card pulls this signal LOW...col. 6, lines 49-52;...the configuration signals ADD_IDo to ADD_ID7 are strapped to high or low depending on the configuration of the ADD card 156...col. 6, lines 60-62;...A detector pin strappable to a logic level to indicate an external graphics card is used...Abstract). Further, Wilen et al. **discloses** on-board and external TMDS/LVDS devices that can drive a flat panel display or a digital display (...the on-board and external TMDS/LVDS devices 140 and 142 are graphic devices that interface to the DVO signaling from the interface port 130. The on-board TMDS/LVDS device 140 is located on the motherboard containing the processor 110 while the external TMDS/LVDS 142 is an add-on card to be plugged into a slot having interface to the interface port 130. The TMDS/LVDS devices 140 and 142 drive a flat panel display or a digital display monitor through a TMDS/LVDS transmitter...col. 3, lines 10-25). Wilen et al. **does not explicitly disclose** wherein the passive loop-through card further comprises a transmission minimized differential signaling (TMDS) transmitter for driving TMDS outputs on DVI signal. However, it would have been obvious to a person of ordinary skill in the art at the time invention was made to make use of TMDS transmitter on a passive loop-through card to preserve the TMDS signal integrity.

f. Regarding claim 23, Wilen et al. **discloses** on-board and external TMDS/LVDS devices 140 and 142 are devices that interface to the DVO signaling from the interface port 130. The on-board TMDS/LVDS device 140 is located on the motherboard containing the processor 110 while the external TMDS/LVDS device 142 is an add-on

card to be plugged into a slot having interface to the interface port 130. The TMDS/LVDS devices 140 and 142 drive a flat panel display or a digital display monitor thorugh a TMDS/LVDS transmitter. The encoder 144 encodes the digital pixel data generated by the graphics controller from the chipset at the chipset space 125 into usable video signal. The television set 146 receives the video signal from the encoder 144 in a suitable format such as NTSC (col. 3, lines 10-25).

g. Regarding claim 48, Wilen et al. **discloses** the interface port 130 including multiplexed pins to support at least two graphics modes (..the interface port 130 provides connection pins to interface to a number of devices. The interface port 130 includes multiplexed pins to support at least two graphics modes...col. 2, lines 62-65). Although, Wilen et al. specifically does not disclose a low and a high voltage level, it would have been obvious to a person of ordinary skill in the art at the time invention was made to make use of multiplexed pins to differentiate the presence of an active graphics card. However, Wilen-Finger combination **does not disclose** a passive loop-through card. The detailed specification of the instant application discloses how the loop-through card 650 completes the circuit paths between the output signals and LVDS panel input signals (paragraph 0030). Kruse et al. **discloses** a flexible interconnect arrangement (FIA) facilitating low voltage differential signal communications between an analyzer and a display screen with a highly flexible, high impedence circuit board (col. 2, line 64-67), which acts as a loop-through card. Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Wilen-Finger combination with the feature "loop-through for passing data" as taught by Kruse et al. **because** it provides for a reduced electromagnetic interference operations resulting in improved operations.

6. Claims 25, 26, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,724,389 B1 to Wilen et al. in view of US 6,202,039 B1 to Finger as applied claim 16 above, and further in view of US 2004/0228365 A1 to Kobayashi.

a. Regarding claim 25, Wilen-Finger combination **is silent about** PCI express signal usage between said graphics processing unit from said integrated graphics processor in order to generate a plurality of signals for display on said output device. Kobayashi **discloses** an add-in graphics card supplanting the onboard graphics engine (See Fig. 23) and use of PCI express port (...the PCI express port is augmented to become compliant with the requirements of the cross platform interface which can directly drive a display device...a add-in graphics card can supplant the onboard graphics engine as shown in Fig. 23...page 9; paragraph 95, 96). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Wilen-Finger combination with the feature "PCI Express technology for communications between on-board and external add-on graphics controllers" as taught by Kobayashi **because** PCI Express is a high-bandwidth, low pin count that maintains software compatibility with existing PCI infrastructure (page 9, paragraph 95).

b. Regarding claim 26, Wilen et al. **discloses** wherein the active graphics card is adapted to generate VGA, TV, LVDS and DVI signals (...the description of invention is directed to the digital video output...the invention can be practiced for other graphic modes...the DVO mode may include a digital video interface (DVI)...or low voltage differential signaling (LVDS)...the television set 146 receives the video signal...col. 2, lines 1-67; col. 3, lines 1-40).

c. Regarding claim 27, it is similar in scope to claims 19 and 21 and is rejected under the same rationale.

7. Claims 28, 29, 30-39, and 49-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,724,389 B1 to Wilen et al. in view of US 7,024,601 B2 to Quinlan et al.

a. Regarding claim 28, Wilen et al. **discloses** a motherboard (computer system 100, Fig. 1); a central processing unit (processor 110, Fig. 1) mounted to the motherboard (computer system 100);an integrated graphics processor (IGP) (on-board accelerated graphics port (AGP) device 150, Fig. 1) mounted to the motherboard (computer system 100); a connector (AGP connector 152, Fig. 1) a field-changeable rendering card (external AGP device 154, Fig. 1) interfaced to the motherboard (computer system 100), wherein the field-changeble graphics card resides in an independent, spaced-apart relation relative to the motherboard (...the external AGP device 154 is an add-on...located externally to the motherboard...The ADD card 156 is a graphics device that interfaces the AGP connector 152...col. 3, lines 34-39). Wilen et al. **discloses** plurality of output display devices such as television output and DVI output. However, Wilen et al. **does not disclose** use of plurality of muxes adapted for interfacing the field-changeble graphics card to a plurality of output display panels. Quinlan et al. **discloses** a digitial visual interface (DVI) that uses plurality of multiplexers (..A block diagram of a digital visual interface (DVI) transmitter 300 circuit is shown in FIG. 3 according to an embodiment of the present invention. The DVI transmitter 300 may comprise the DVI transmitter 104 shown in FIG. 1. The DVI transmitter 300 is coupled to receive digital red data, digital green data, and digital blue data representing digital visual information. The digital red data is to be coupled to a display unit to generate red color in a visual image, the digital green data is to be coupled to the display unit to generate green color in the visual image, and the digital blue data is to be coupled to the display unit to generate blue color in the visual image. The visual image is displayed by the display

unit...The line 318 is coupled to transmit encoded and serial red data between the serializers 316 and a first multiplexer 330. The line 320 is coupled to transmit encoded and serial green data between the serializers 316 and a second multiplexer 332. The line 322 is coupled to transmit encoded and serial blue data between the serializers 316 and a third multiplexer 334. Each of the multiplexers 330, 332, and 334 is a type of multiplexer known to those skilled in the art...col. 4, lines 48-64; col. 5, lines 22-28). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Wilen et al. with the feature "plurality of muxes adapted for interfacing graphics card to a plurality of output display panels" as taught by Quinlan et al. **because** it provides for high level control of selecting an output display rather than a resistor stuffing option thus providing flexibility and user-friendly interface.

b. Regarding claim 29, Wilen et al. **discloses** a connector (AGP connector 152, Fig. 1) for attaching field-changeable graphics card (...the external AGP device 154 is an add-on...located externally to the motherboard...The ADD card 156 is a graphics device that interfaces the AGP connector 152...col. 3, lines 34-39) (external AGP device 154, Fig. 1) to the motherboard (computer system 100), the connector comprising a plurality of connector pins (...The AGP connector 152 is a connector that supports the AGP standard (e.g., version 2.0)...col. 3, lines 25-35).

c. Regarding claim 30, it is similar in scope to claim 18 above and is rejected under the same rationale.

d. Regarding claim 31, it is similar in scope to claim 19 above and is rejected under the same rationale.

e. Regarding claim 32, it is similar in scope to claim 20 above and is rejected under the same rationale.

f. Regarding claim 33, it is similar in scope to claim 21 above and is rejected under the same rationale. Quinlan et al. **discloses** use of plurality of muxes (col. 4, lines 48-64; col. 5, lines 22-28). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Wilen et al. with the feature "plurality of muxes adapted for interfacing graphics card to a plurality of output display panels" as taught by Quinlan et al. **because** it provides for high level control of selecting an output display rather than a resistor stuffing option thus providing flexibility and user-friendly interface.

g. Regarding claim 34, it is similar in scope to claim 22 above and is rejected under the same rationale.

h. Regarding claim 35, it is similar in scope to claim 23 above and is rejected under the same rationale.

i. Regarding claim 36, it is similar in scope to claim 24 above and is rejected under the same rationale.

j. Regarding claim 37, Wilen et al. **does not disclose** plurality of muxes adapted to automatically reconfigure to receive and transmit signals from the active graphics card. Quinlan et al. **discloses** use of plurality of muxes (col. 4, lines 48-64; col. 5, lines 22-28). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Wilen et al. with the feature "plurality of muxes adapted for interfacing graphics card to a plurality of output display panels" as taught by Quinlan et al. **because** it provides for high level control of selecting an output display rather than a resistor stuffing option thus providing flexibility and user-friendly interface.

k. Regarding claim 38, it is similar in scope to claim 25 above and is rejected under the same rationale.

l. Regarding claim 39, it is similar in scope to claim 26 above and is rejected under the same rationale.

m. Regarding claim 49, it is similar in scope to claim 53 above and is rejected under the same rationale.

n. Regarding claim 50, it is similar in scope to claim 44 above and is rejected under the same rationale.

o. Regarding claim 51, it is similar in scope to claim 45 above and is rejected under the same rationale.

p. Regarding claim 52, it is similar in scope to claim 46 above and is rejected under the same rationale.

q. Regarding claim 53, it is similar in scope to claim 47 above and is rejected under the same rationale.

r. Regarding claim 54, it is similar in scope to claim 4 above and is rejected under the same rationale.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Dalip K. Singh** whose telephone number is **(571) 272-7792**. The examiner can normally be reached on Mon-Friday (10:00AM-6: 30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Ulka Chauhan**, can be reached at **(571) 272-7782**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private

PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Please note that the new Central Official FAX number for application specific communications with the USPTO is **571-273-8300** (effective July 15, 2005).

Dalip K. Singh

Examiner, Art Unit 2628

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September 27, 2006

ULKA CHAUHAN
SUPERVISORY PATENT EXAMINER